AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A processor, comprising:

at least one interface engine comprising a microcode memory and being adapted to be connected to at least one external device located externally of the processor; and

a programmable pipeline adapted to directionally transfer data packets through the pipeline from a first end of the pipeline to a second end of the pipeline, and adapted to perform sequences of instructions on the data packets,

the pipeline comprising plural pipeline stages and plural access points, the pipeline stages and the access points being arranged in a row between the first end of the pipeline and the second end of the pipeline, the access points providing the at least one external device with access to the pipeline, at least one of the access points separating and connecting two of the pipeline stages,

wherein the at least one interface engine is connected to the plural access points,

wherein the at least one interface engine is adapted to:

~~i) to~~ receive a request from any one of the connected access points of the programmable pipeline, the request being received upon arrival of one of the data packets at the respective any one access point, the request comprising a first request code, according to a first coding scheme adapted for the processor,

execute a microcode program stored in the microcode memory, the execution of the microcode program being dependent upon the first request code, to obtain, as a result of the execution of the microcode program, at least one device control code according to a second coding scheme adapted for the external device, wherein the execution of the microcode program being dependent upon the first request code in that the start address of the microcode program corresponds at least partly to the first request code,

generate at least one request output, the at least one request output being based at least partly on the request from the one access point and/or at least partly on the device control code,

~~ii) to~~ send [[a]] at least one request output to the external device, ~~the request output being based at least partly on the request from the one access point,~~

~~iii)~~ receive, responsive to the request output, ~~to receive~~ an external reply from the external device, and

~~iv) to~~ send to the pipeline a response, based on the external reply, to the request, and

wherein the interface engine includes an arbiter configured to allow forwarding of requests from the connected access points in a fair manner between each of the connected access points~~, reducing risks of delays in the directionally transfer of data packets through the pipeline~~.

2. (canceled)

3. (original) A processor according to claim 2, whereby the device control code is an operational code of the external device.

4. (canceled)

5. (previously presented) A processor according to claim 1, the interface engine comprising a reply control unit adapted to receive at least one receiver ID signal related to the request, and to determine, based on the receiver ID signal, the access point which is to receive the response.

6. (previously presented) A processor according to claim 5, whereby the reply control unit is adapted to receive an input control signal, and timing information for receiving the

external reply from the external device is determined from the input control signal.

7. (previously presented) A processor according to claim 1, whereby the number of access points adapted to send a request to the interface engine is adjustable.

8. (currently amended) A method in a processor comprising a programmable pipeline and at least one interface engine comprising a microcode memory, the interface engine being adapted to be connected to at least one external device located externally of the processor, the processor being adapted to directionally transfer data packets through plural pipeline stages from a first end of the pipeline to a second end of the pipeline, the pipeline comprising a plurality of access points located in a spaced-apart relation separating and connecting two pipeline stages and between the first end of the pipeline and the second end of the pipeline, the at least one interface engine being connected to the plurality of access points and allowing the at least one external device access to the pipeline stages via the access points, the interface engine comprising an arbiter configured to allow forwarding of requests from the plurality of access points in a fair manner between each of the plurality of access points, the method comprising the steps of:

receiving a request from any one of the connected access points of the programmable pipeline, the request being received upon arrival of a data packet at the respective any one access point, the request comprising a first request code, according to a first coding scheme adapted for the processor;

executing, by means of the interface engine, a microcode program stored in the microcode memory, the execution of the microcode program being dependent upon the first request code, to obtain, as a result of the execution of the microcode program, at least one device control code, according to a second coding scheme adapted for the external device, wherein the execution of the microcode program being dependent upon the first request code in that the start address of the microcode program corresponds at least partly to the first request code;

generating at least one request output, the at least one request output being based at least partly on the request from the one access point and/or at least partly on the device control code;

sending [[a]] the at least one request output to the external device, ~~the request output based at least partly on the request from the one access point,~~

~~responsive to the request output,~~ receiving, responsive to the at least one request output, an external reply from the external device, and

sending to the pipeline a response, based on the external reply, to the request.

9. (canceled)

10. (previously presented) A method according to claim 9, whereby the device control code is an operational code of the external device.

11. (canceled)

12. (previously presented) A method according to claim 8, further comprising the steps of:

sending at least one receiver ID signal, related to the request, to a reply control unit included in the interface engine, and

determining, based on the receiver ID signal, the access point which is to receive the response.

13. (previously presented) A method according to claim 12, further comprising the step of sending to the reply control unit an input control signal, wherein timing information for receiving the external reply from the external device is determined from the input control signal.

14. (previously presented) A method according to claim 8, whereby the number of access points adapted to send a request to the interface engine is adjustable.

15. (previously presented) A processor according to claim 1, wherein the fair manner of the arbiter is a round-robin manner between the plurality of access points.

16. (previously presented) A method according to claim 8, wherein the fair manner of the arbiter is a round-robin manner between the plurality of access points.

17. (currently amended) A processor, comprising:

a programmable pipeline comprised of plural pipeline stages and access points located between a first end of the pipeline and a second end of the pipeline,

the access points providing ~~the at least one external device with~~ access to the pipeline to at least one external device,

at least some of the access points separating and connecting an adjacent two of the pipeline stages, and

the pipeline configured to directionally transfer data packets from the first end to the second end; and

an interface engine[[,]]comprising a microcode memory, having a reply control unit, and connected to an external device

located externally of the processor, and connected to the plurality of access points, the interface engine configured to

~~i)~~ receive a request from the pipeline upon arrival of a data packet at any one of the connected access points, the request comprising a first request code, according to a first coding scheme adapted for the processor,

execute a microcode program stored in the microcode memory, the execution of the microcode program being dependent upon the first request code, to obtain, as a result of the execution of the microcode program, at least one device control code according to a second coding scheme adapted for the external device, wherein the execution of the microcode program being dependent upon the first request code in that the start address of the microcode program corresponds at least partly to the first request code,

generate at least one request output, the at least one request output being based at least partly on the request from the one access point and/or at least partly on the device control code,

~~ii)~~ send [[a]] the at least one request output to the external device, ~~the request output based at least partly on the request,~~

~~iii) responsive to the request output,~~ receive, responsive to the at least one request output, an external reply from the external device, and

~~iv)~~ send a response, based on the external reply, to the pipeline,

and the reply control unit configured to

i) receive a receiver ID signal related to the request, and

ii) determine, based on the receiver ID signal, the any one of the plurality of access points of the pipeline to receive the response.

18. (previously presented) A processor according to claim 17, wherein a quantity of the plurality of access points from which the request is received by the interface engine from the pipeline is adjustable based on one of

i) a data flow rate through the pipeline, and

ii) a flow capacity of the external device.

19. (previously presented) A processor according to claim 17, wherein the interface engine includes an arbiter configured to allow forwarding of requests from the plurality of access points in a fair manner between each of the plurality of access points.

20. (previously presented) A method according to claim 19, wherein the fair manner of the arbiter is a round-robin manner between the plurality of access points.